UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,831	12/30/2003	Kevin M. Conley	0084567-247US0	9380

66785 7590 01/14/2010

DAVIS WRIGHT TREMAINE LLP - SANDISK CORPORATION
505 MONTGOMERY STREET
SUITE 800
SAN FRANCISCO, CA 94111

EXAMINER	
ELAND, SHAWN	

ART UNIT	PAPER NUMBER
2185	

MAIL DATE	DELIVERY MODE
01/14/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/749,831
Filing Date: December 30, 2003
Appellant(s): CONLEY ET AL.

Gerald P. Parsons
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 06/22/09 appealing from the Office action mailed 12/22/08.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US 2002/0099904	Conley	07-2002
US 2002/0034105	Kulkarni	03-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 2-4, 28, 29, 31, 32, 34, 36, 38 and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by ***Conley*** (US PG Publication 2002/0099904 A1).

As for claim 2, Conley teaches a method of writing data into a non-volatile memory system of a type having blocks of a minimum number of memory cells that are simultaneously erasable and which individually store a given number of host units of data, comprising:

designating a first of the blocks for storage of a number of units of data with sequential logical addresses that is less than a pre-set proportion of the given number, the pre-set proportion being less than the given number, thereafter responding to a plurality of successive host commands to write a number of units of data less than the pre-set proportion of the given number that have sequential logical addresses by writing their data into a first designated block, and responding to host commands to write a number units of data having sequential logical addresses equal to or in excess of the pre-set proportion of said given proportion of said given number by writing their data into a block other than the first designated block **(paragraph 0062, all lines – the storage capacity of a block is determined as to indicate if the amount of data to be stored is equal to or less than/greater than the capacity of the block. If the capacity is sufficient, the system will try to put the data in a partially written block. If not, the system will address a new block and store the within this block, or across multiple blocks based on the data size – see also Fig. 14. Figs. 8 and 9 further illustrate Conley as physically storing data in a sequential manner (i.e. contiguous pages))**.

To help illustrate this point, assume *arguendo*, that "a number of units of data" (hereinafter given number) is equal to the storage capacity of one of Conley's entire blocks, and that "a pre-set proportion" equals 100% of said given number. Conley's system, determines that a number of writes equal to or greater than said given number could not be written to a partial written block (e.g. first designated block), hence the data would be written to a block other than the first designated block. Also, if the amount of data to be written is less than 100% the capacity of a full block, and there is enough space to write that amount of data to a partially written block, Conley would write that number of units less than 100% of said given number to a

partially written block (e.g. first designated block) in accordance with the flow illustrated in Fig. 14 of Conley.

In regard to claim 28, Conley teaches a method of writing data into a non-volatile memory system of a type having blocks of a minimum number of memory cells that are simultaneously erasable and which individually store a given number of host units of data, comprising:

designating at least a first one of the blocks to store a number of units of data having sequential logical addresses that is less than a pre-set fraction of said given number **(as stated in the rejection of claim 2, the partially written block (as discussed in figure 14) is the first block)**.

thereafter responding to a plurality of successive host commands to individually write units of data into the memory system by determining whether a number of the units of data with sequential logical addresses is less than the pre-set fraction, and, if so, by writing the data into the first designated block, and responding to host commands to write units of data having a number of sequential logical addresses that is equal to or in excess of the pre-set fraction of said given number by writing the data into a block other than the first dedicated block **(paragraph 0062, all lines – the storage capacity of a block is determined as to indicate if the amount of data to be stored is equal to or less than/greater than the capacity of the block. If the capacity is sufficient, the system will try to put the data in a partially written block. If not, the system will address a new block and store the within this block, or across multiple blocks based on the data size – see also Fig. 14. Figs. 8 and 9 further illustrate Conley as physically storing data in a sequential manner (i.e. contiguous pages))**.

To help illustrate this point, assume *arguendo*, that "a number of units of data" is equal to the storage capacity of one of Conley's entire blocks, and that "a pre-set fraction" equals 100% of said given number. Conley's system, determines that a number of writes equal to or greater than said given number could not be written to a partial written block (e.g. first designated block), hence the data would be written to a block other than the first designated block. Also, if the amount of data to be written is less than 100% the capacity of a full block, and there is enough space to write that amount of data to a partially written block, Conley would write that number of units less than 100% of said given number to a partially written block (e.g. first designated block) in accordance with the flow illustrated in Fig. 14 of Conley.

As for claim 31, Conley teaches a method of operating a non-volatile memory system in response to commands received from a host to individually write logically addressed units of data therein, the memory system having memory cells grouped into blocks of a minimum number of memory cells that are simultaneously erasable and which individually store a given number of units of data at individual physical addresses, the logical addresses of received units of data being mapped within the memory system into corresponding physical addresses where the received units of data are stored, comprising:

allocating a first one of the blocks to store units of data having a number of sequential logical addresses less than a fraction of said given number **(Fig. 14, elements 52, 53, 61, 63 – paragraph 0062 – if the system determines that enough space is available to accommodate the amount of data required by the pages corresponding to a number of logical addresses, the data will be allocated to the partially written block)**,

allocating a second one of the blocks to store units of data having a number of sequential logical addresses equal to or in excess of the fraction of said given number **(Fig. 14, elements 52, 53, 55 – paragraph 0062 – if the system determines if a sufficient amount of space is not available to accommodate the amount of data required by the pages corresponding to the number of logical addresses, a second block (new erased block) will be allocated to store the data)**,

in response to receipt of a command to write data having a number of sequential logical addresses less than said fraction, determining whether the first block has sufficient erased capacity to store the received data and, if so, writing the received data into sequential physical addresses of the first block **(Fig. 14, elements 61 and 67 – paragraph 0062 – once the system determines that enough pages are available in the partially written block (i.e. element 61), the data will be written into the newly allocated block (element 67))**, and

in response to receipt of a command to write data having a number of sequential logical addresses equal to or in excess of said fraction, determining whether the second block has erased capacity to store the data and, if so, writing the data into sequential physical addresses of the second block **(Fig. 14, elements 55 and 57 – paragraph 0062 – once the system determines that a new erased block is sufficient to store the data, the new data is written to the block (element 57))**.

As for claim 32, Conley teaches,

in response to receipt of the command to write data having a number of sequential logical addresses less than said fraction, if the first block does not have sufficient erased capacity to store the received data, allocating a third one of the blocks to store units of data having a number

of sequential logical addresses less than a fraction of said given number and then writing the received data into sequential physical addresses of the third block **(Fig. 14, elements 65 and 67 – paragraph 0062 – once the system determines that the partial block is not large enough, a new erased block (third) will be allocated and written to)**, and

in response to receipt of the command to write data having a number of sequential logical addresses equal to or in excess of said fraction, if the second block does not have sufficient erased capacity to store the received data, allocating a fourth one of the blocks to store units of data having a number of sequential logical addresses equal to or in excess of the fraction of said given number and then writing the received data into sequential physical addresses of the fourth block **(Fig. 14, elements 55 and 57 – paragraph 0062 – once the system determines that a one new erased block is not sufficient to store the data, an additional block (i.e. fourth) will be allocated to accommodate the new data (elements 55 and 57))**.

As for claim 3, Conley teaches determining whether or not the successive host commands individually include a number of units of data having sequential logical addresses less than the pre-set proportion of said given number **(referring again to paragraph 0062, and the rejections stated above, the given number is based on the size of an entire block)**.

As for claims 4, 29 and 34, Conley teaches the non-volatile memory cells as being organized into multiple sub-arrays, and said blocks of memory cells include memory cells of two or more of the sub-arrays **(paragraph 0062, all lines, if the amount of host data does not exceed the size of one full block the data, two different sets of host writes can be stored uniquely in one block (i.e. each write is a unique sub-array of data within each block). Also**

note Conley specifically teaches his memory system as including sub-arrays in paragraph 0010, lines 1-7).

As for claim 36, Conley teaches a method of writing data into a non-volatile memory system of a type having blocks of a minimum number of memory cells that are simultaneously erasable and which individually store a given number of host units of data, comprising:

designating at least a first one of the blocks to store a number of units of data received by the memory system with individual ones of multiple write commands that have sequential logical addresses less than a pre-set fraction of said given number **(as stated in the rejection of claim 2, the partially written block (as discussed in figure 14) is the first block)**,

responding to the receipt of multiple commands by the memory system to individually write one or more units of data thereinto by, for individual commands **(data is written to the memory in accordance with the host's commands)**,

(a) determining whether the command specifies the writing of a number of units of data having sequential logical addresses that is less than the pre-set fraction **(paragraph 0062, all lines – the system determines the amount of data to write)**, and (b) determining whether the first block has enough erased capacity to store the number of units of data provided with the command **(figure 14, partial blocks are checked to determine if enough capacity is available to store the data before data is either stored in partial block, or to a new one/s)**, wherein

when both of conditions (a) and (b) above are determined to exist, thereafter writing the units of data into the first block **(paragraph 0062, all lines – if less than a**

full block is to be written, and there is enough space in the partially written block, the data will be written to the partially written block), but

when either one of conditions (a) or (b) above is determined not to exist, writing the units of data into one of the blocks other than the first block **(if more data than one the size of one block is to be written or the partial block lacks the capacity to store the entire set of data is written to the new block – figure 14)**.

As for claim 38, Conley teaches:

designating at least a second one of the blocks to store a number of units of data received by the memory system with individual ones of multiple write commands that have sequential logical addresses equal to or greater than the pre-set fraction **(figure 14, element 55, the newly addressed block will store the data)**, and

responding to the receipt of multiple commands by the memory system to individually write one or more units of data thereinto by additionally, for individual commands **(the system will follow the flow illustrated in Fig. 14 for the commands transmitted by the host)**,

(c) determining whether the command specifies the writing of a number of units of data greater than the given number **(Fig. 14, element 53)**, wherein when neither of the conditions (a) nor (c) above exist, writing the units of data into the second block, without regard to whether condition (b) exists or not, but when the condition (c) above is determined to exist, writing the units of data into one of the blocks other than the first or second blocks **(again, (if more data than one the size of one block is to be written or**

the partial block lacks the capacity to store the entire set of data is written to the new block – Fig. 14).

As for claim 40, Conley teaches a non-volatile memory system having memory cells grouped into blocks of a minimum number of memory cells that are simultaneously erasable and which individually store a given number of units of data at individual physical addresses, the logical addresses of received units of data being mapped within the memory system into corresponding physical addresses where the received units of data are stored, a method of operation in response to received commands to individually write logically addressed units of data therein, comprising:

designating a first one of the blocks to store units of data having a number of sequential logical addresses less than a pre-determined fraction of said given number **(as stated in the rejection of claim 2, the partially written block (as discussed in figure 14) is the first block)**,

designating a second one of the blocks to store units of data having a number of sequential logical addresses equal to or in excess of the fraction of said given number **(newly addressed block – Fig. 14, element 55)**,

providing at least another one of the blocks that is fully erased **(Fig. 14, element 57, a block or multiple blocks will be provided depending on the size of the data)**, and

in response to receipt of a command to write data into the memory system, identifying the number of units of the data that have sequential logical addresses, determine whether the number of such units with sequential logical addresses are less than the fraction **(Fig. 14, element 53)**, and, if so,

writing the data to the first of the blocks **(if enough capacity exists in the partially written block, the data will be written in the partial block)**, but if the amount of data is not less than the fraction, then

writing the data to the second of the blocks if there is sufficient capacity therein, but if there is not sufficient capacity in the second of the blocks, writing the data to the fully erased block **(if the partially written block does not have enough space the data will be first written to a newly addressed block, and additional blocks if the additional capacity is required 0 Fig. 14, elements 53, 55, and 57)**.

Claims 26, 27, 30, 33, 35, 37, 39, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Conley*** (US PG Publication 2002/0099904 A1) as applied to claims 2 and 28 above, and in further view of ***Kulkarni*** et al. (Us PG Publication 2002/0034105 A1), hereinafter ***Kulkarni***.

As for claims 26, 27, 30, 33, 35, 37, 39 and 41, though Conley teaches all the limitations of claims 2 and 28, he fails to specifically teach the pre-set proportion as being set within a range of 25-75 percent of the given number as recited by Applicant in these claims.

Kulkarni however teaches a system and method for incrementally updating an image in flash memory wherein new flash images are built incrementally until a memory block is of sufficient size to be written to the flash memory – paragraph 0013, all lines. More specifically, Kulkarni teaches writing memory to a first memory block (i.e. RAM), until the memory is half

full (i.e. 50 percent), and subsequently writing the data to a second block in the flash memory (i.e. predetermined limit set at 50% allocation) – paragraph 0014, all lines.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Conley to further include Kulkarni's system for updating an image in flash memory into his own system for partial block data programming in a non-volatile memory. By doing so, Conley would have a more efficient memory system capable for reducing the number of sections transmitted during the writing process, while persevering sections that are used to construct other section as taught by Kulkarni in paragraph 0011, all lines. Additionally, Conley could benefit from Kulkarni's system by preventing the problems related to data overwrite as described by Kulkarni in paragraph 0012, all lines.

(10) Response to Argument

Appellant argues:

The Examiner's interpretation of "proportion" is contrary to the way the term is used in the present application.

Examiner response:

The term proportion, by itself can mean 100%, as that's the full proportion of something. 200% is a double portion. A "preset proportion" by itself is also just as ambiguous as it only "presets" the proportion. It does not limit the size of the proportion. Without any further qualifiers in the claim language the Examiner can use any ratio as he sees fit. The Examiner was

merely arguing against Appellant's statement that proportion can never mean 100%. It is the addition of "the pre-set proportion being less than the given number of units" into the claim language that further limits the claims. Of this, the Appellant and Examiner agree. However, this doesn't change the fact that Conley still writes data to a block, said data being smaller than the block (for example, figure 14, steps 52, 53, 61, and 65) and thus partially fills a block.

Appellant argues:

Claims 2 and 28 call for applying a plurality of programming commands for receiving a number of units of data with successive commands, instead of using Conley's single command.

Examiner response:

Conley checks the ability of a partial block fill with every incoming command. If multiple commands with partial block data come from the host, then Conley does not break down. Conley is very flexible in this regard.

Appellant argues:

It is not clear that Kulkarni discloses filling up its non-volatile memory blocks to only 50% of their capacity.

Examiner response:

There appears to be a contradiction in the Appellant's argument. The Appellant states, starting on line 2 of page 10 of the Appeal brief (filed 06/22/09), that "Kulkarni only states that the 50% point is when data are then written from the RAM into the non-volatile memory." As stated in the last Office action, the RAM block corresponds to the non-volatile blocks in size. When you

write (i.e. fill) a block that is 50% in RAM, you fill your non-volatile block at 50%. Finally, it should also be noted that Kulkarni is used in conjunction with Conley as a 35 U.S.C. 103 rejection and it is the part of first writing to RAM and then moving the partially filled data to the non-volatile memory.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Shawn Eland/

Examiner, Art Unit 2185

Conferees:

/Kevin L Ellis/
Supervisory Patent Examiner, Art Unit 2117